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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,171	06/18/2002	James W. Adkisson	BUR919990299	8362

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,171	ADKISSON ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 18-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,18 and 20-22* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION
Drawings

1. Drawing changes indicated in annotated marked up copies in Letter of August 4, 2004 are acknowledged and deemed to be acceptable.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 18, and 20 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Battersby et al. (US 5,528,065) in view of Liao (US 6,180,477 B1).

4. Regarding Claim 1, Battersby et al. disclose a dual gate FET semiconductor device comprising a conduction channel (under gate 11, Figure 5) of first width and a dual gate of dimension <<100 mm (Col. 6, lines 48 – 50) (x-axis in figure) with source/drain regions (5,6) (Col. 4, line 53) located at opposite ends of a monocrystalline conduction channel, and self-aligned (Col. 1, line 64 through Col. 2, line 2) polysilicon (Col. 7, lines 47 – 48) gate regions on opposing sides of said conduction channel (Figure 5), wherein the smallest feature (insulated gate sections, 11,12) of said field effect transistor is formed through a lithographic process and of a second width, wherein, said first width (channel) is smaller than said second width (Col. 6, lines 24 – 39) (See Figure 5, wherein channel width is smaller than gate).

Battersby et al. do not disclose the presence of silicide sidewalls on polysilicon gate regions and on a surface containing source and drain regions, wherein the source-drain resistance is reduced. Liao discloses silicide sidewalls (222) (Figure 2D) (Col.3, lines 33 – 37) formed "on" polysilicon gate region (204) and "on" a surface wherein source/drain regions are formed, wherein source-drain resistance is reduced. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the procedures of Liao with Battersby et al. to obtain a reduction in breakdown of the FET.

5. Regarding Claim 2, Battersby et al. do not disclose the presence of silicide sidewalls in the form of liners. As discussed above, Liao discloses silicide sidewalls (222) (Figure 2D) (Col.3, lines 33 – 37) formed "on" polysilicon gate region (204) and "on" a surface wherein source/drain regions are formed, thereby forming a liner ("jacket or coating").

6. Regarding Claim 18, Battersby et al. disclose that the long dimension (width) of the conduction channel (Col. 9, lines 16 – 17) exceeds the first width (length) (distance between source and drain) (Col. 9, lines 14 – 16) by a factor of more than four times (Col. lines 26 – 29).

7. Regarding Claim 20, Battersby et al. disclose an insulating material (at 11, 12) between said source and drain regions where said polysilicon is recessed (Figure 5).

8. Regarding Claim 21, Battersby et al. disclose that the source/drain (5-5a,6-6b) regions and said conduction channel (at 16) are formed in monocrystalline silicon "on" an insulator (gate oxide), wherein said source/drain regions have a width greater than said conduction channel.

9. Regarding Claim 22, Battersby et al. disclose that the field oxide (4) can be formed by local oxidation (Col. 7, lines 30 – 33) to form a shallow "trenched" isolation region, wherein the device structure is repetitive (Figure 4) and the isolation regions are between source and drain regions.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Battersby et al. in view of Liao and Adan et al., as applied to Claims 1, 2, 18, and 20 – 22, and further in view of Mizuno et al. (US 5,844,278).

11. Regarding Claim 3, Battersby et al. do not disclose that the polysilicon gate regions are connected by a connector. Mizuno et al. disclose that the polysilicon gate regions are connected with a polysilicon strip at the top (See Figure 17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Mizuno et al. with Battersby et al. to obtain a working device with interconnection structure.

12. Claims 4 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Battersby et al. in view of Liao, Mizuno et al., and Adan et al., as applied to Claims 1 – 3, 18, and 20 –

22, above, and further in view of Liu et al. (US 6,380,078 B1).

13. Regarding Claims 4 and 5, Battersby et al. do not disclose that the connector is a damascene connector. However, Liu et al. disclose a method for forming damascene interconnects (See Figure 2F) wherein trenches are formed in an insulating layer, filled with metal, and the surface planarized (Col. 8, lines 47 – 54). It would have been obvious at the time of the invention to one of ordinary skill in the art to use the method of Liu et al. to form damascene interconnects between gates and to combine with Liu et al. with Battersby et al. and Liao to reduce the delay associated with resistance and capacitance of the interconnect structure.

14. Regarding Claims 6 – 8, Battersby et al. do not disclose that the silicide sidewalls are connected or that the connector is a damascene connector formed within a trench in the insulating region. However, Liu et al. disclose a method for forming damascene interconnects (See Figure 2F) wherein trenches are formed in an insulating layer, filled with metal, and the surface planarized (Col. 8, lines 47 – 54). It would have been obvious at the time of the invention to one of ordinary skill in the art to use the method of Liu et al. to form damascene interconnects and to combine Liu et al. with Battersby et al., and Liao to reduce the delay associated with resistance and capacitance of the interconnect structure.

Claim Objections

15. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims. The prior art of record do not reasonably teach or suggest, either singularly or in combination, the limitation of *"a conduction channel [with] a width of approximately 5 nm."*

Response to Arguments

16. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

In regard to commentary on the use of Liu et al., Examiner notes that there is no recitation by Applicant of sub-lithographic dimensions in the relevant claims, and Liu et al. is appropriate.

Conclusions

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
October 12, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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